Appendix B
Details of Timing Analysis Report

This Appendix explains some of the concepts involved in static timing analysis. After design implementation, the timing analyses reports are used to assess the design's system performance, which is limited by seven basic types of timing paths. This information is collected from the Xilinx ™ Manual for the Timing Analyzer tool.

The timing paths go through a sequence of routing and logic. These sequences can vary, since these path delays are affected by the results of the placement and routing that implement the design connectivity. In the following subsections we list each of the timing paths and explain it.

B.1 Clock to Setup

The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs. When these flip-flops are clocked by the same clock, the delay on this path is equivalent to the cycle time of the clock. The Figure B.1 shows a clock-to-setup path which uses the same clock. Figure B.1 also shows a timing diagram describing the path.

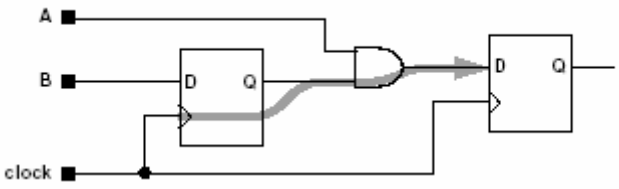

Figure B.1 Clock-to-Setup Path

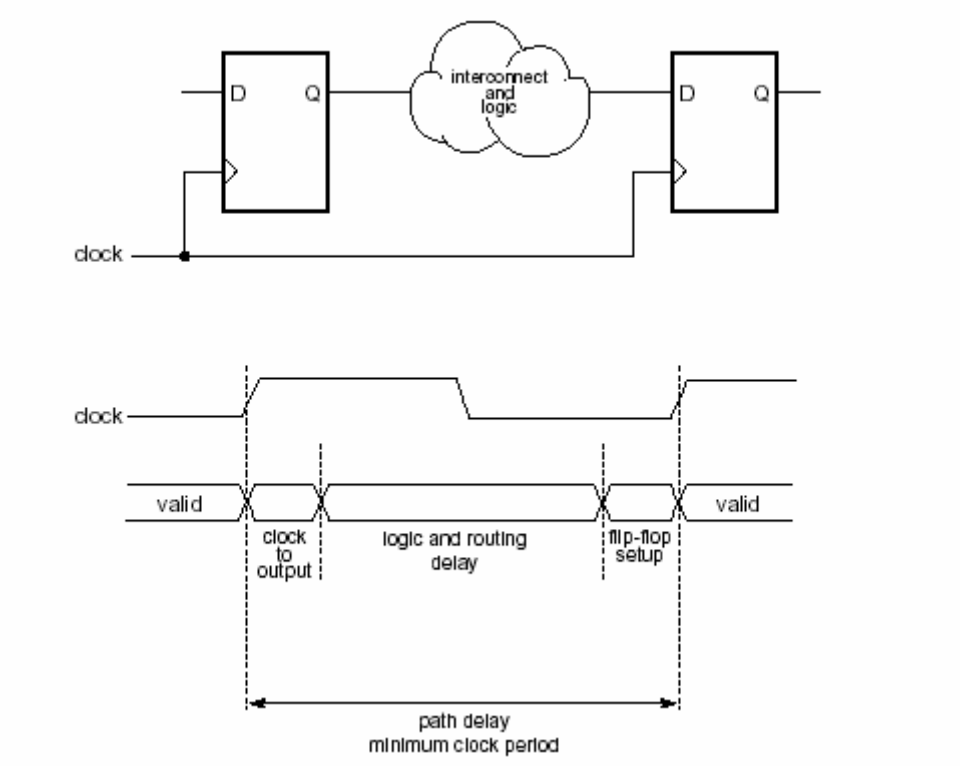

Figure B.2 Clock to Setup Path with Timing Diagram

B.2 Clock to Pad

The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and leave the chip. Figure B.3 illustrates a clock-to-pad path, while Figure B.4 demonstrates the clock-to-pad path along with a timing diagram describing the path.

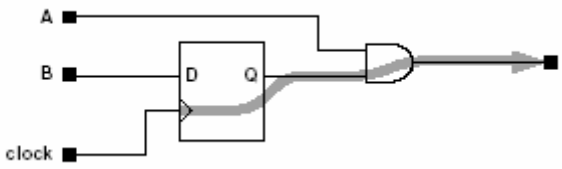

Figure B.3 Clock to Pad Path

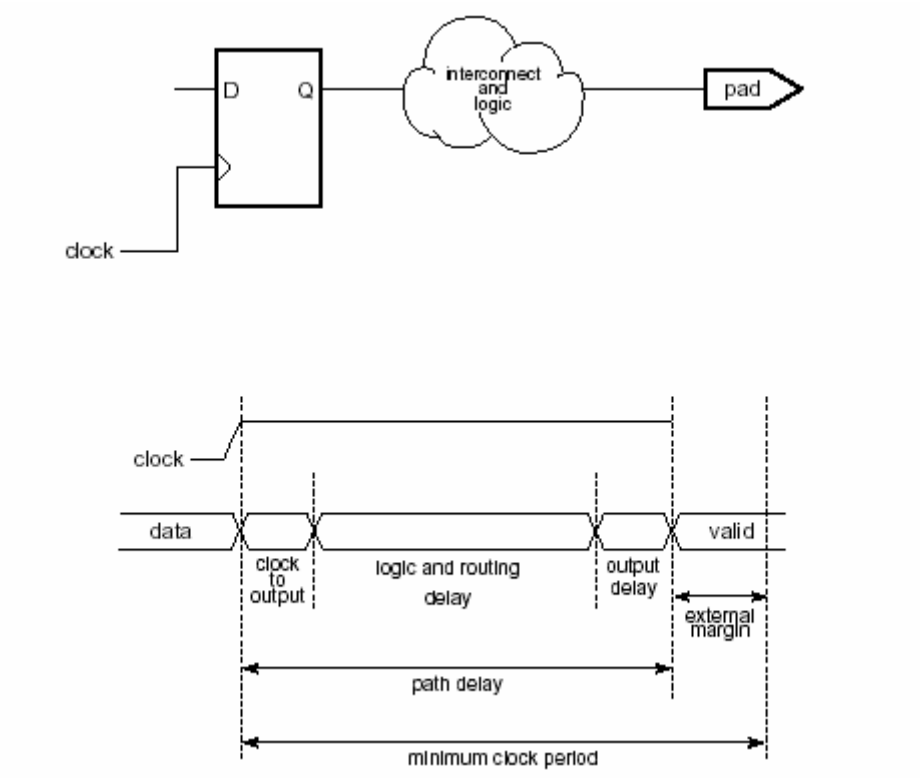

Figure B.4 Clock to Pad Path with Timing Diagram

B.3 Paths Ending at Clock Pin of Flip Flops

The clock input path time is the maximum time required for the clock signal to arrive at the flip-flop clock input propagating through any number of levels of combinatorial logic. Clock input paths help to determine system-level design timing. Figure B.5 shows the clock path delay in the case of the existence of some combinatorial logic between the clock source and the input clock pin.

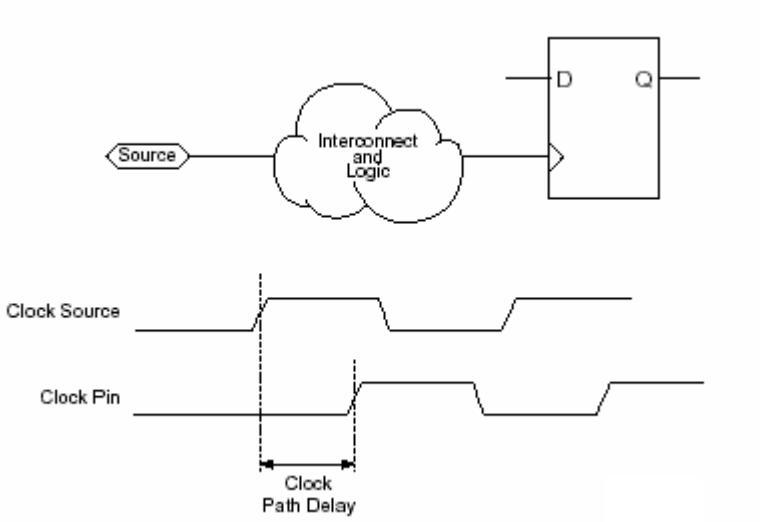

Figure B.5 Clock Path Delay with Timing Diagram

B.4 Setup to Clock at the Pad

The clock path delay reports t_{SU} for data inputs relative to "global" or "product term" clock inputs. It is calculated according to the following formula for global and product term clocks.

t_{SU} = Pad to Setup - Path Ending at Clock Pin of Flip-Flop

E B.1

Global clock paths start at global clock pads, propagate through global clock buffers and end at a flip-flop clock pin. Product term clock paths start at input pads, propagate through a single level of logic implemented in a clock product term, and end at the flip-flop clock pin. The last two clock-at-the-pad paths are shown in Figure B.6.

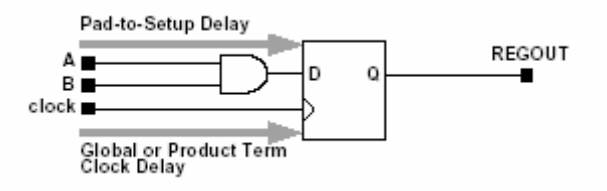

Figure B.6 Clock at the Pad Paths

B.5 Clock Pad to Output Pad

A clock-pad-to-output-pad path starts at input pads and trace through all paths that include a flip-flop clock input before ending at an output pad. That path breaks when it includes a flip-flop asynchronous set or reset input. Clock-pad-to-output-pad paths trace through tri-state controlled pad enable inputs.

B.6 Pad to Pad

The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal. A pad-to-pad path, along with a timing diagram describing the path is displayed in Figure B.7, while in Figure B.8 the path is described with a timing diagram.

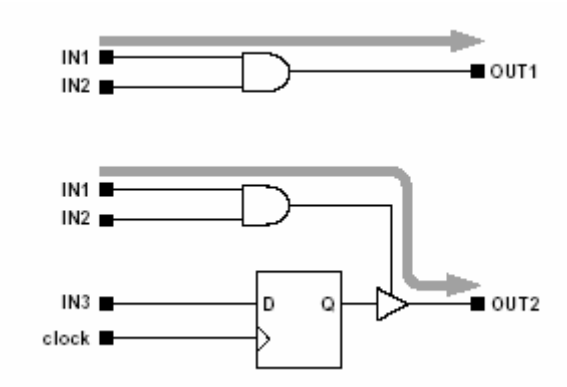

Figure B.7 Pad to Pad Path

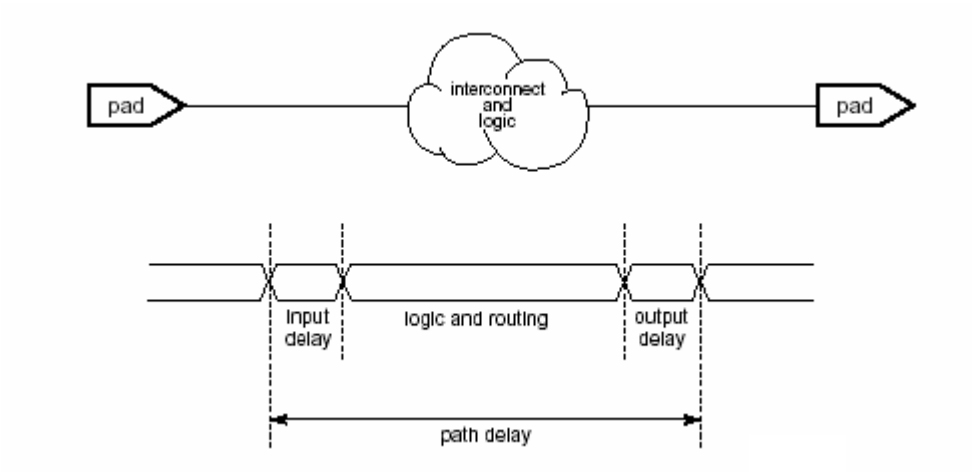

Figure B.8 Pad to Pad Delay with Timing Diagram

B.7 Pad to Setup

The pad-to-setup path time is the maximum time required for the data to enter the chip, travel through logic and routing, and arrive at the output before the clock or control signal arrives. A pad-to-setup path and timing diagram is shown in the following figure.

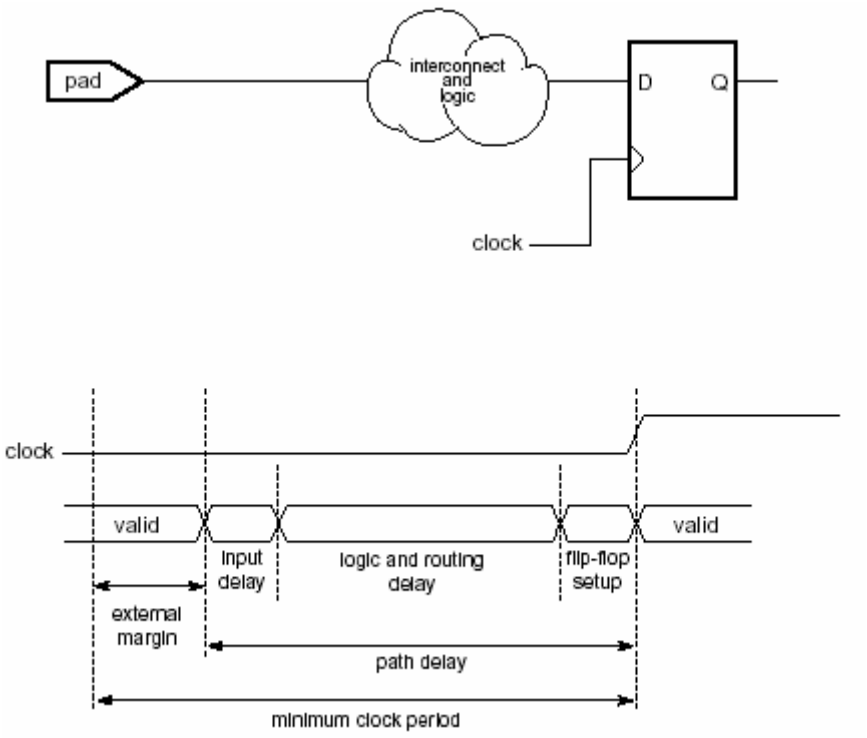

Figure B.9 The Pad to Setup Delay with Timing Diagram