Arab Academy for Science, Technology & Maritime Transport
School of Engineering
Computer Department
Computing Systems (CC 513)

Midterm No. 2 **Time: 90 minutes**
May., 2007 **Lecturer: Prof. Dr. Magdy Saeb**
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Student Name: …… **ID number:** ……

Answer only four of the following problems:

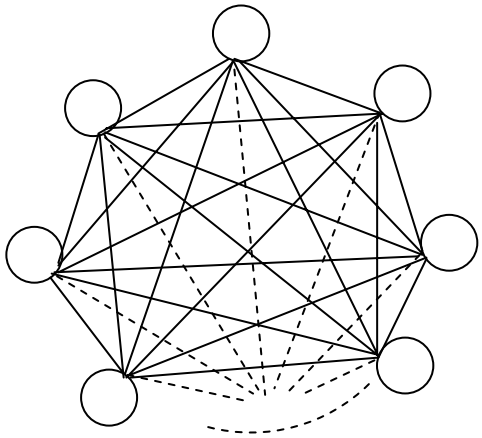
Problem 1: ***25 points***

Consider the following sequence of instructions, where the syntax consists of an opcode followed by the destination register followed by one or two source registers.
These instructions are expected to run on a superscalar machine that can handle two instructions at a time at each stage and allow out-of-order execution. Each pipeline consists of four stages: fetch, decode/issue, execute, write-back. Assume that all pipeline stages take one clock cycle except for the execute stage. For simple integer arithmetic and logical instructions, the execute stage takes one cycle, but for a LOAD from memory, five cycles are consumed in the execute stage.
Construct the following table for the execution of the six instructions and state the reason for delays, if they exist, in any stage.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
ADD R3,R1,R2																			
LOAD R6,[R3]																			
AND R7,R5,3																			
SUB R6, R5,R1																			
OR R2, R4, R7																			
ADD R0, R1, R8																			

Problem 2: ***25 points***

a. Consider the following fully-connected interconnection topology, what is the node degree, network diameter, bisection width and the cost for a network of size N?
b. If the delay d between any two processing-nodes is the same, compute the average inter-processor delay.

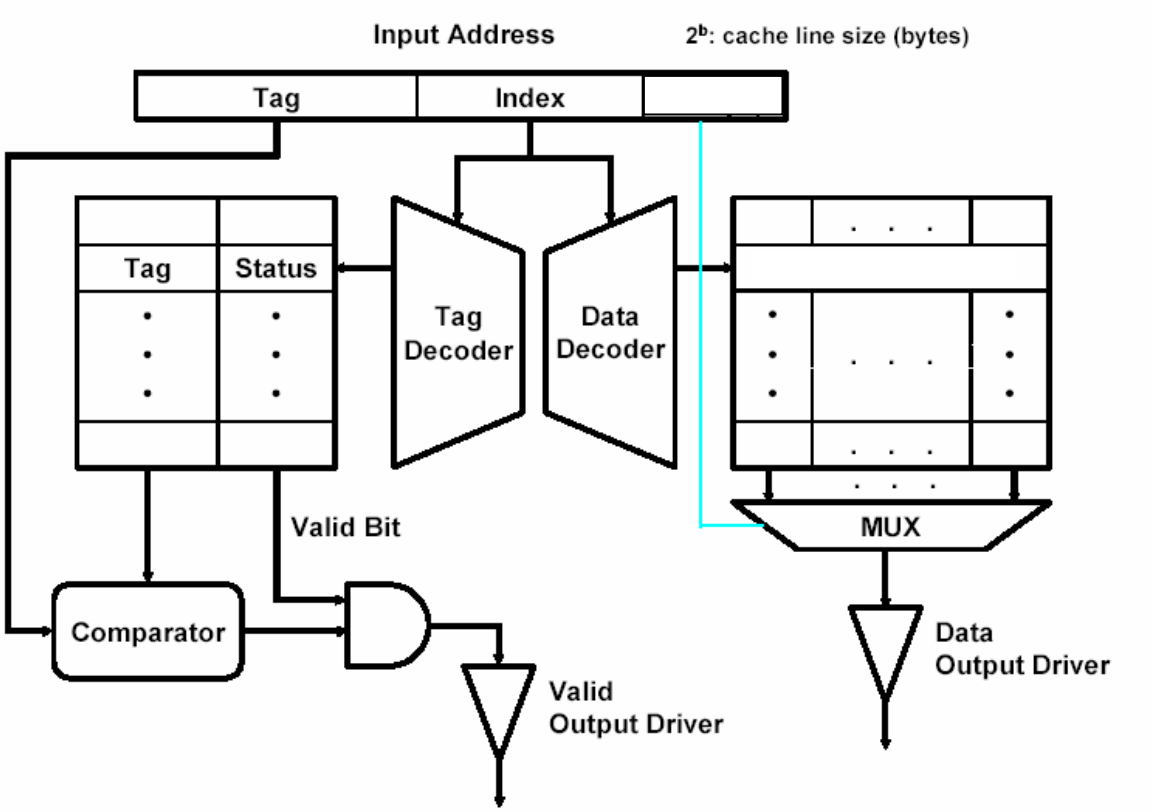


Answer:

Problem 3: ***25 points***

Consider a 2-MB cache with 32-byte cache lines. The address is 27 bits, and the cache access is byte-aligned. The data output is also 8 bits, and the MUX selects one byte out of the 64-bytes in a cache line.

a. Fill in the table for the direct-mapped (DM) cache shown in figure, using the delay equations given in the table below. Assume that two bits are reserved for the "Status" field and that the delay for the two-input AND gate is 500 psec.
b. Show the critical path in the following hardware and compute the memory access time in pico seconds.
c. If the processor to which this cache memory will be coupled works at 300MHz, how many cycles would one memory access require?



Component	Delay equation (ps)		DM (ps)
Decoder	200×(# of index bits) + 1000	Tag	
		Data	
Memory array	200×$\log_2$ (# of rows) + 200×$\log_2$ (# of bits in a row) + 1000	Tag	
		Data	
Comparator	200×(# of tag bits) + 1000		
N-to-1 MUX	500×$\log_2$ N + 1000		
Data output driver	500×(associativity) + 1000		
Valid output driver	1000		

Problem 4: ***25 points***

Given the processor throughput in instructions per nano second G versus the number of segment partitions S as follows:

$$G = \frac{Performance}{\Delta t}$$

$$G = \frac{1}{(1 + b(S-1))} * \frac{1}{(1+k)\frac{T}{S} + C}$$

Where, b is the frequency of interruptions due to incorrectly guessed or unexpected branches, k is the stretching factor that accounts for clock skew, 0<= k<=1.0, T is the total time in ns, C is the fixed clock over head.

a. Show that the optimum value of the number of segments partitions to maximize the processor throughput is given by:

$$S_{opt} = \sqrt{(1-b)(1+k)\frac{T}{bC}}$$

b. Now get S_{opt} given that T = 100 ns, b= 0.20, C = 5 ns, k= 0.125. Also, find G_{max}.

Answer:

Problem 5: ***25 points***

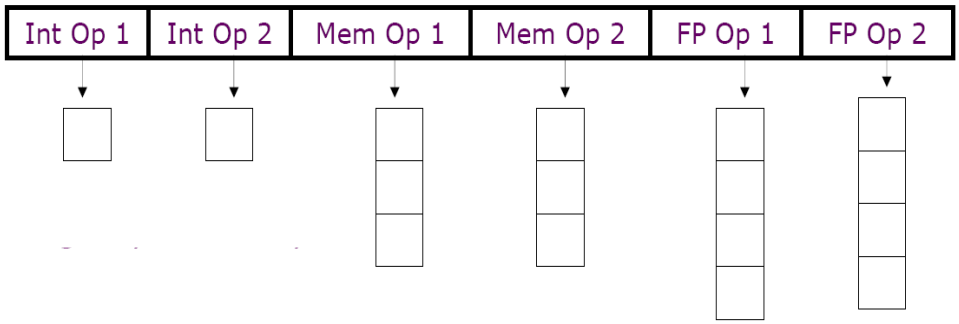
5.1 Compare VLIW architectures with superscalar architectures.
a) Show the similarities and differences
b) Show the advantages and disadvantages of the two approaches.

5.2 Consider a sequence of eight instructions and show how it passes through a four and six-stage pipeline respectively. Draw a figure for each of the two cases.
How many clock cycles are needed in each case?
Assuming that the second machine cycle time is 0.8 times the cycle time of the first machine.
Which is the shorter execution time of the sequence?
Can we conclude that increasing number of stages always provides improved performance? Bring arguments. (Consider that no hazards occur).

Problem 6: ***25 points***

6.1 a) Regarding Flynn's classification of computer architectures; give the definition of the alternative architectures and draw a block diagram for each one.
b) Discuss at least three types of interconnection networks, and draw a diagram for each one. What are the advantages and disadvantages of each type?

6.2 Explain in detail, the type of the machine that supports such operation(s).
Specify each operation in detail and the number of cycles for all operations if the first two operations are performed in one cycle each.



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