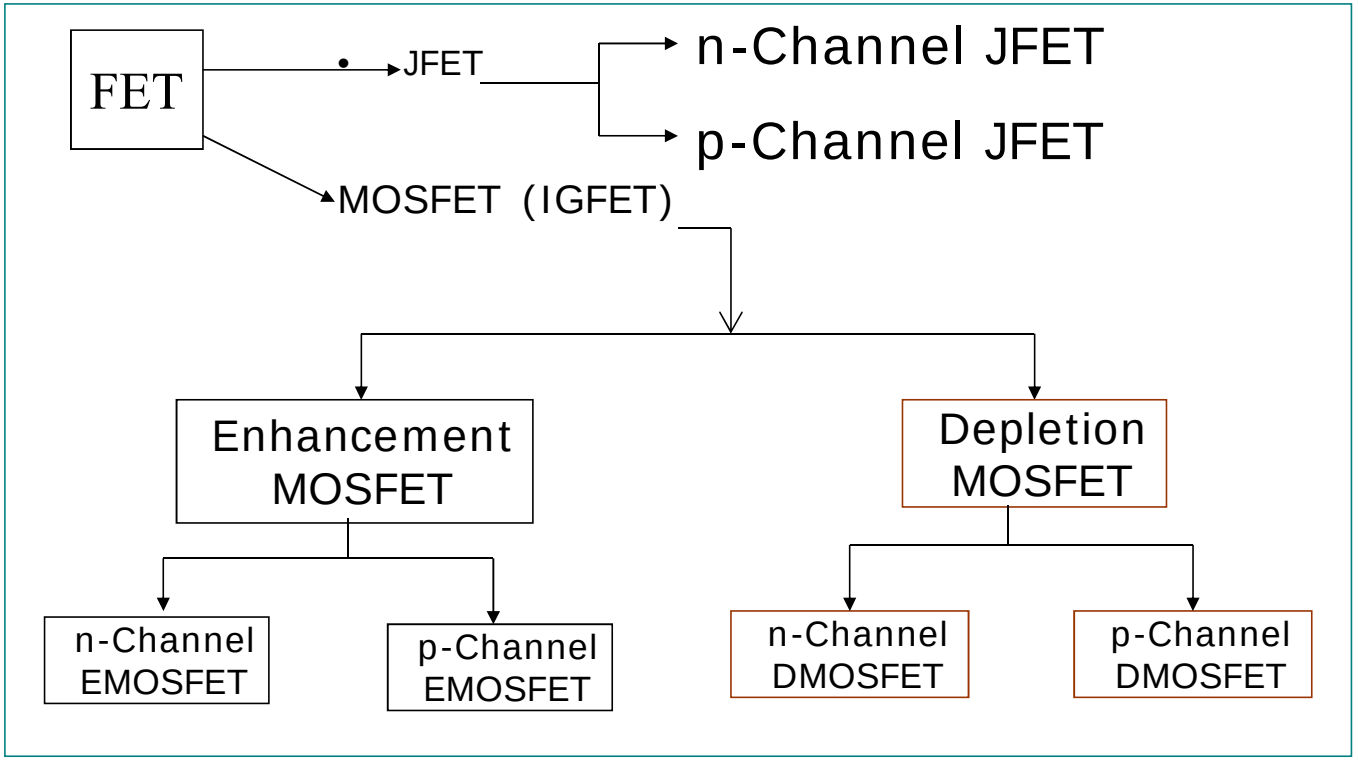
The Junction Field Effect Transistor (JFET)

FET (The Field Effect Transistor)

Few important advantages of FET over conventional Transistors

1. Unipolar device i. e. operation depends on only one type of charge carriers (*h* or *e)*
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance ($\approx 10^9$-$10^{12}\ \Omega$)
4. Source and drain are interchangeable in most Low-frequency applications
5. Low Voltage Low Current Operation is possible (Low-power consumption)
6. Less Noisy as Compared to BJT
7. No minority carrier storage (Turn off is faster)
8. Self limiting device
9. Very small in size, occupies very small space in ICs
10. Low voltage low current operation is possible in MOSFETS
11. Zero temperature drift of out put is possiblek

Types of Field Effect Transistors (The Classification)



The Junction Field Effect Transistor (JFET)

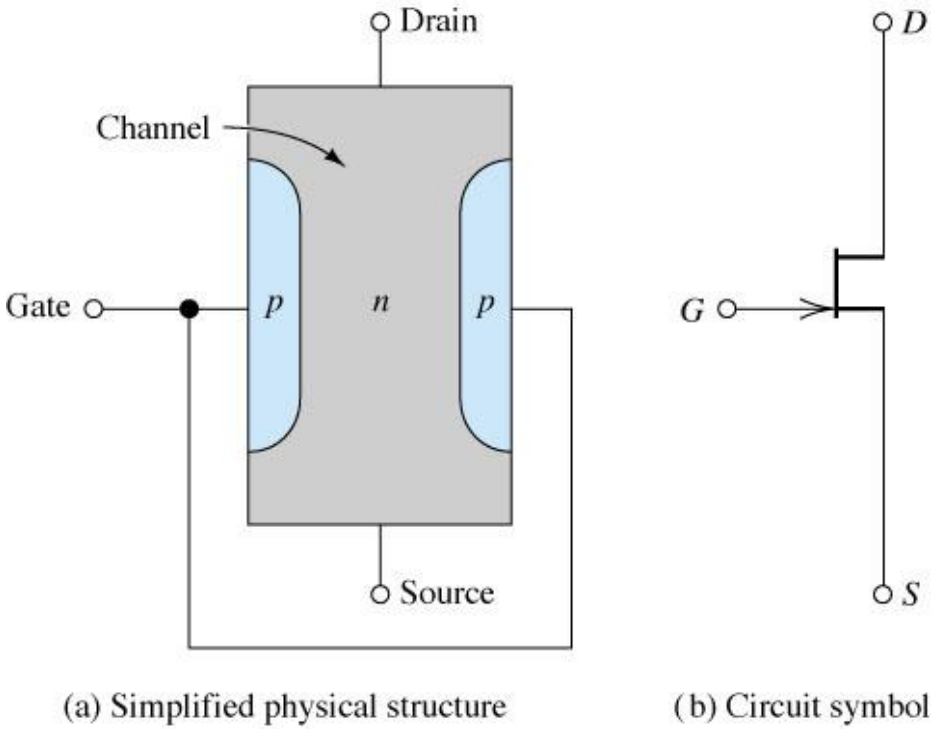
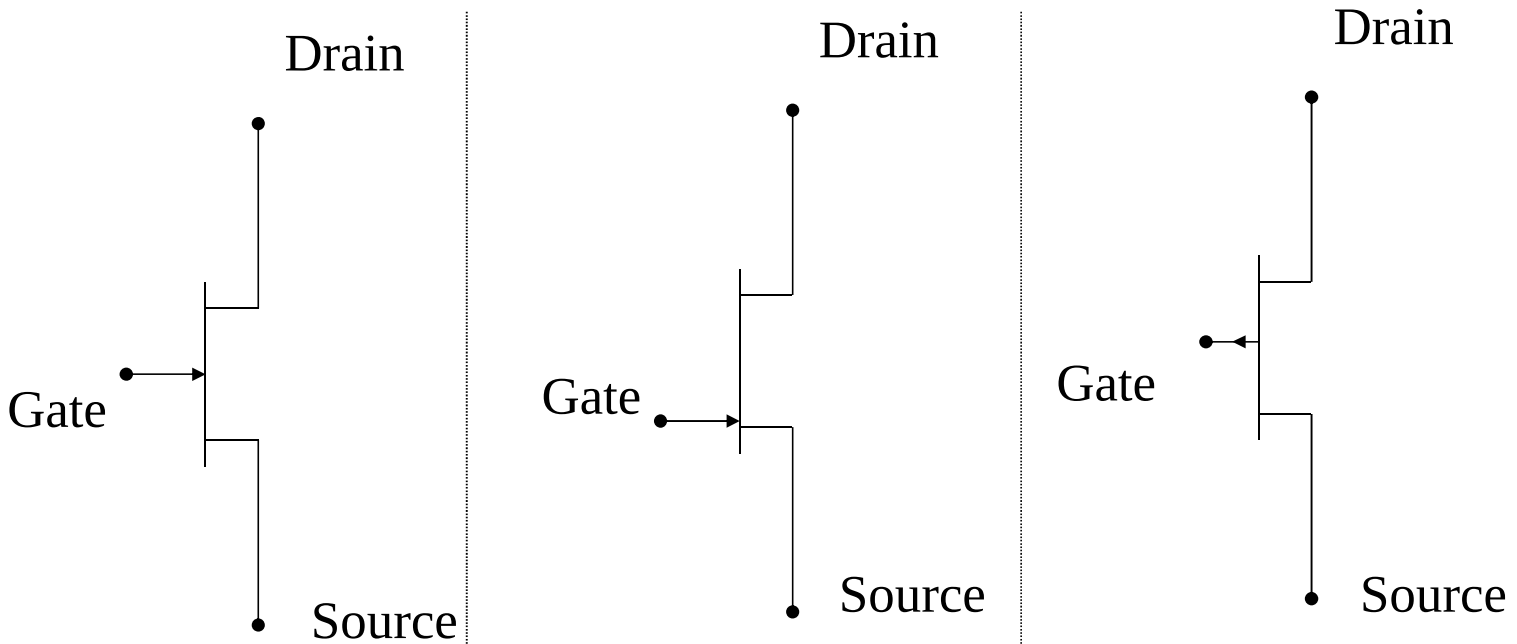


Figure: *n*-Channel JFET.

SYMBOLS


Drain
Gate
Source
n-channel JFET
Drain
Gate
Source
n-channel JFET
Offset-gate symbol
Drain
Gate
Source
p-channel JFET

Biasing the JFET

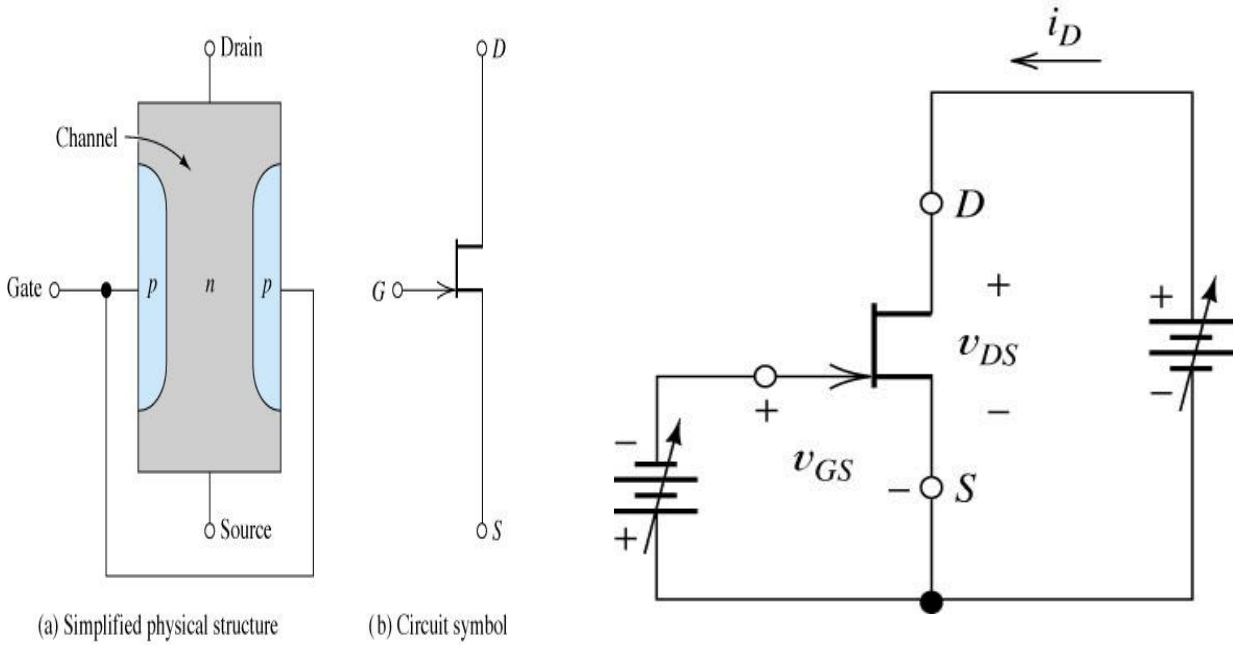
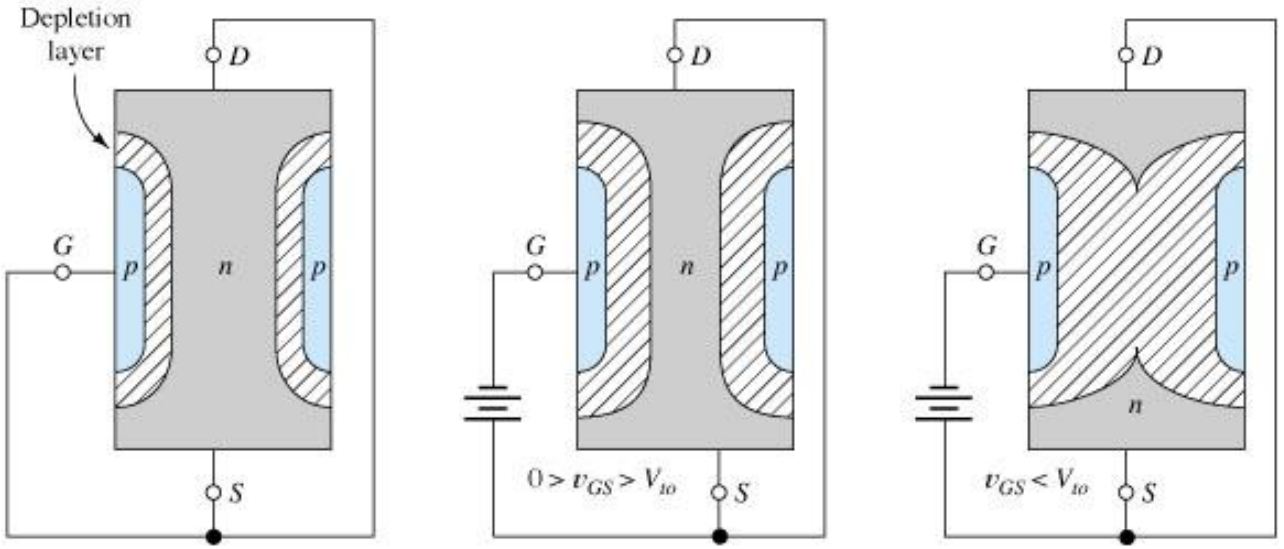


Figure: *n*-Channel JFET and Biasing Circuit.

Operation of JFET at Various Gate Bias Potentials



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

Figure: The nonconductive depletion region becomes broader with increased reverse bias. (*Note:* The two gate regions of each FET are connected to each other.)

Output or Drain (V_D-I_D) Characteristics of n-JFET

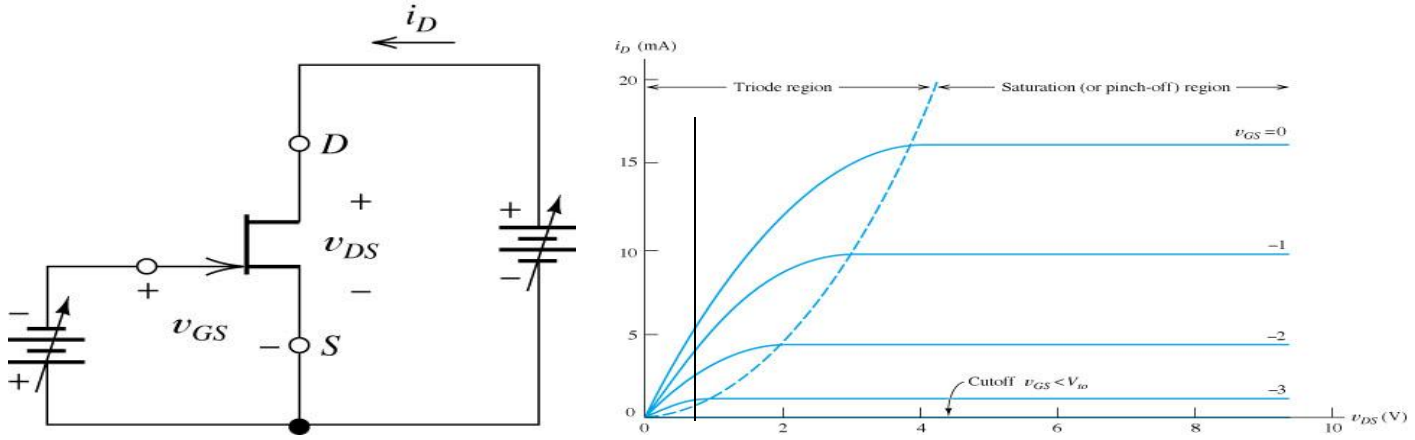


Figure: Circuit for drain characteristics of the *n*-channel JFET and its Drain characteristics.

Non-saturation (Ohmic) Region: $\rightarrow$ $V_{DS} < \left(V_{GS} - V_P\right)$

The drain current is given by $I_{DS} = \frac{2 I_{DSS}}{V_P^2}\left[\left(V_{GS} - V_P\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$

Saturation (or Pinchoff) Region: $\rightarrow$ $V_{DS} \geq \left(V_{GS} - V_P\right)$

$I_{DS} = \frac{I_{DSS}}{V_P^2}\left[\left(V_{GS} - V_P\right)^2\right]$ and $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Where, I_{DSS} is the short circuit drain current, V_P is the pinch off voltage

Simple Operation and Break down of n-Channel JFET

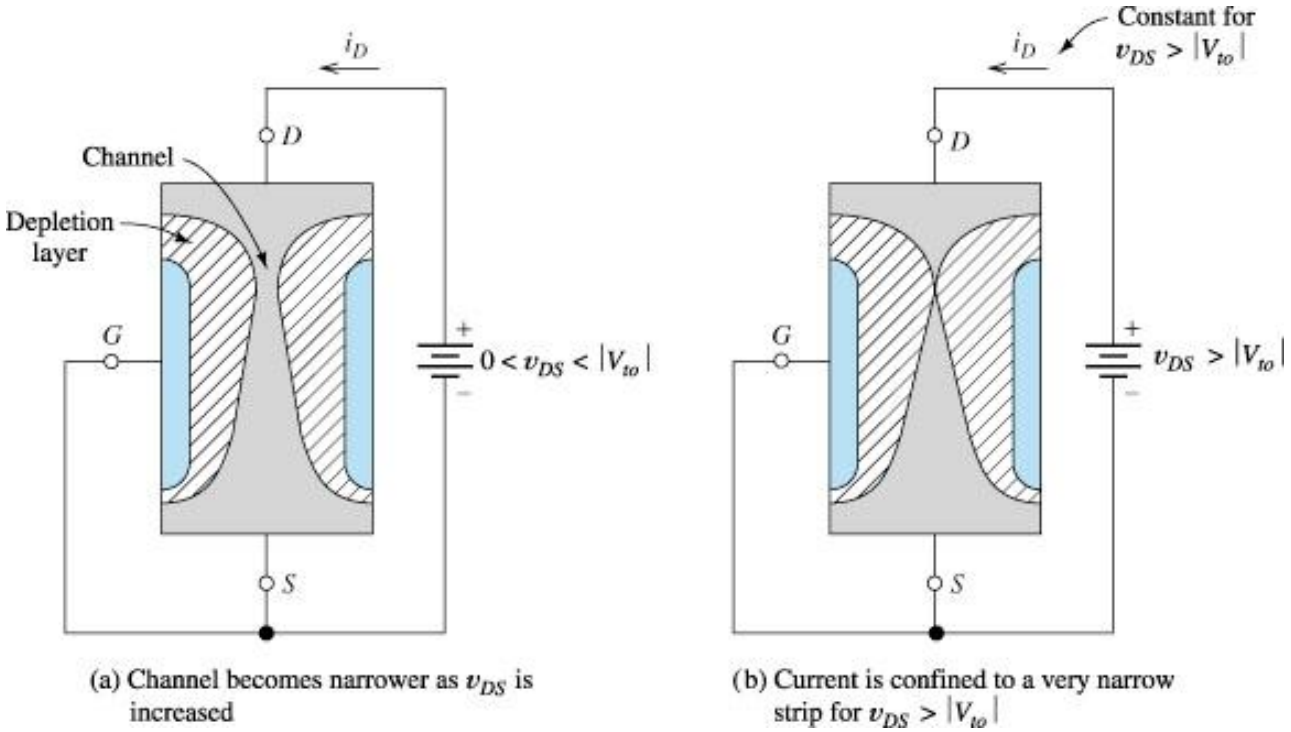


Figure: *n*-Channel FET for $v_{GS} = 0$.

N-Channel JFET Characteristics and Breakdown

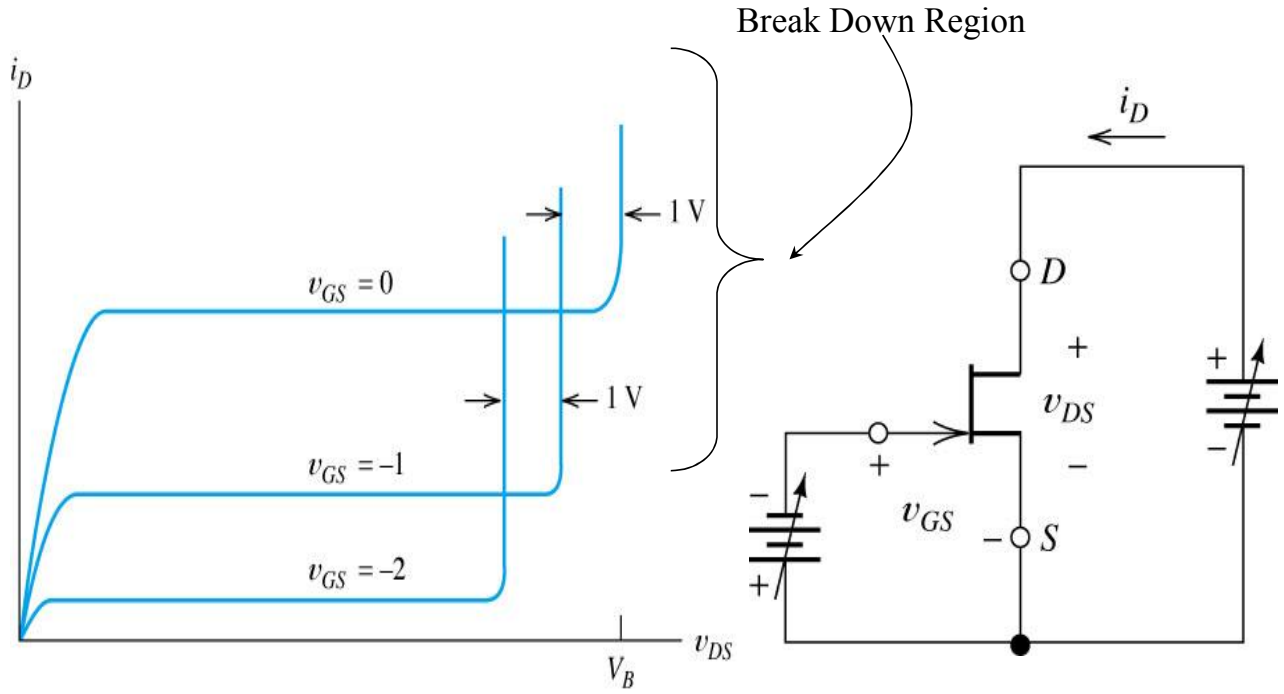
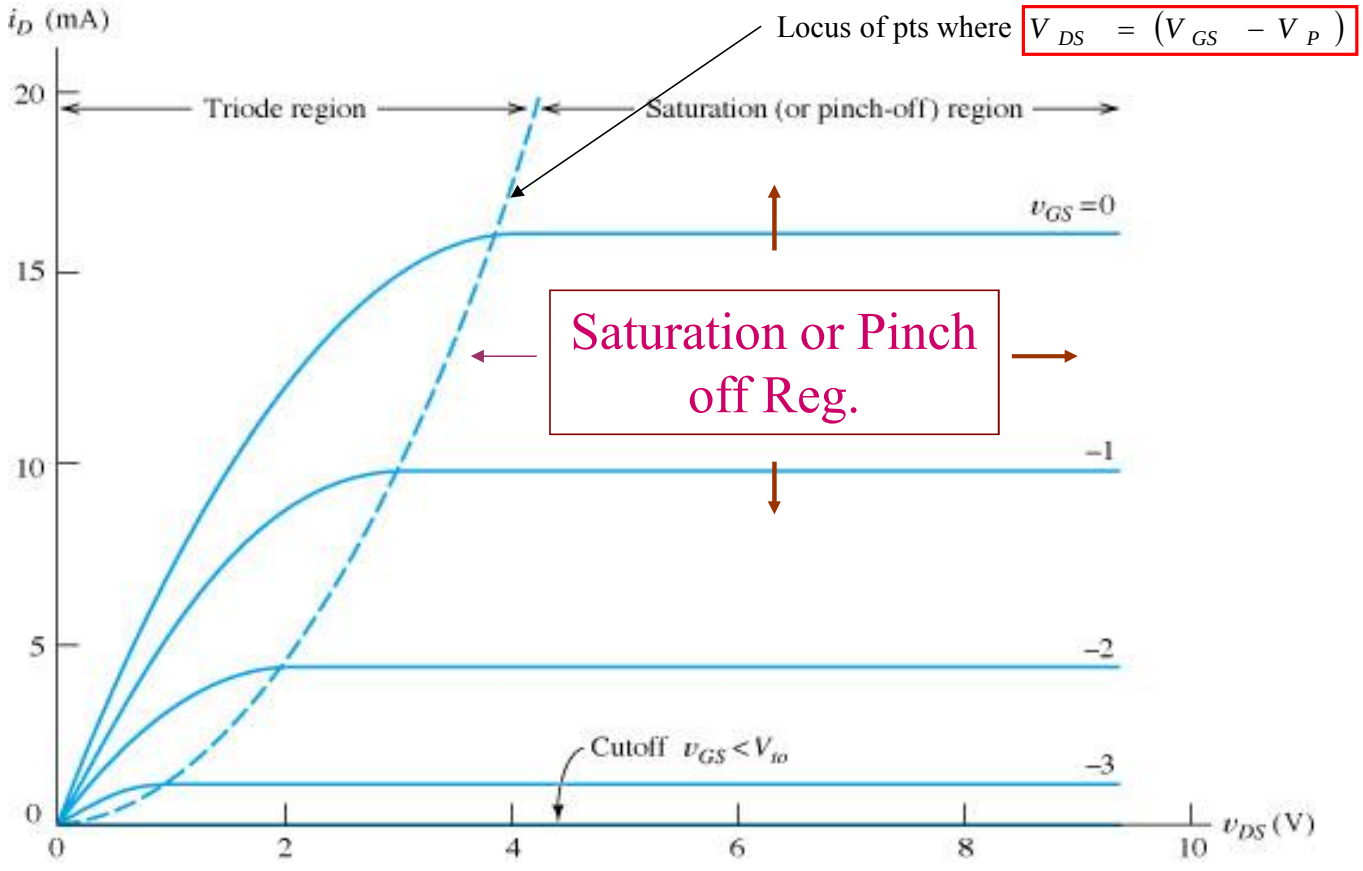


Figure: If v_{DG} exceeds the breakdown voltage V_B, drain current increases rapidly.

V_D-I_D Characteristics of FET



The Transfer (Mutual) Characteristics of n-Channel JFET

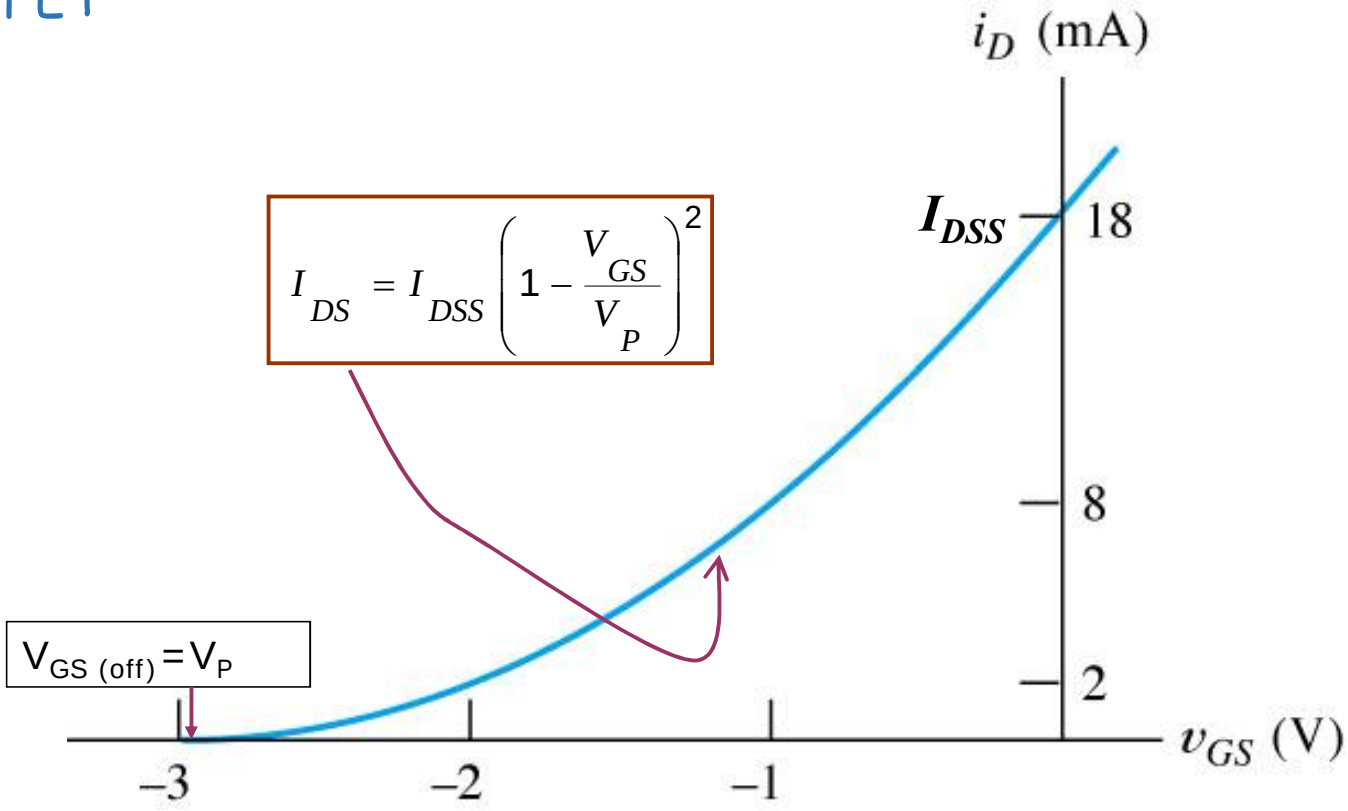
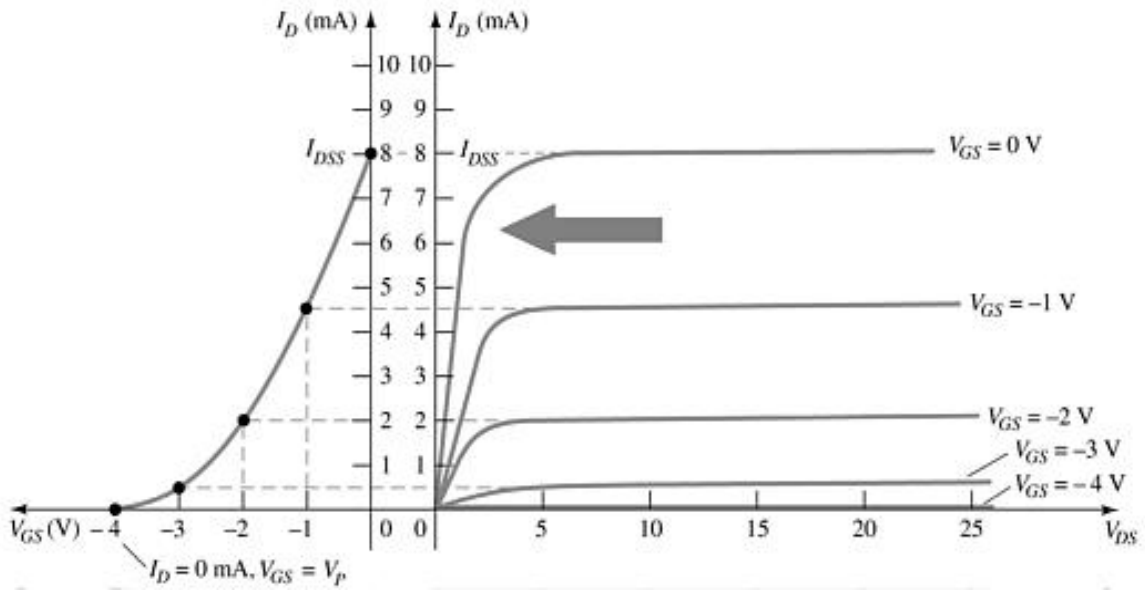


Figure: Transfer (or Mutual) Characteristics of n-Channel JFET

The JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}

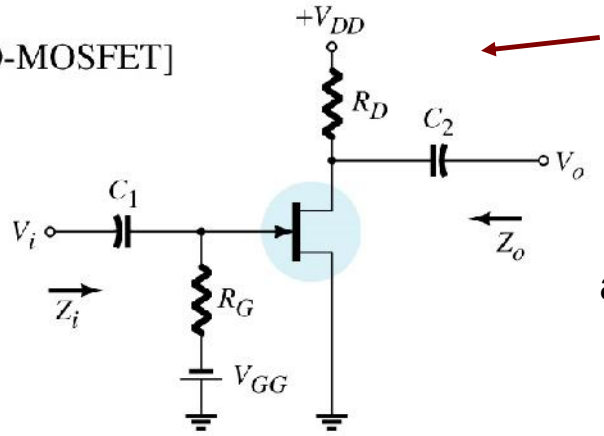


Biasing Circuits used for JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

JFET (n-channel) Biasing Circuits

Fixed-bias
[JFET or D-MOSFET]



For Fixed Bias Circuit

Applying KVL to gate circuit we get

$$V_{GG} = I_G R_G + V_{GS} = V_{GS} = Fixed, \because I_G = 0$$

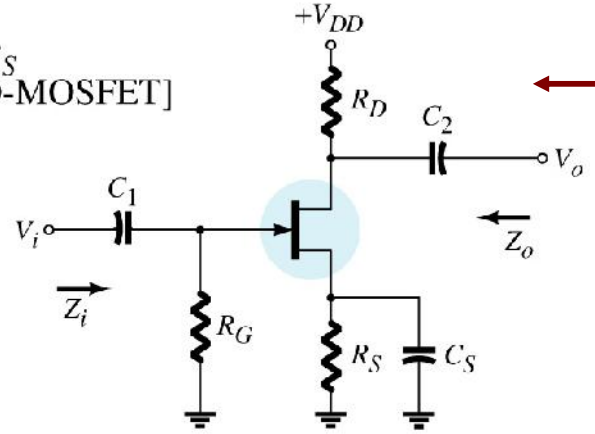
and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and $V_{DS} = V_{DD} - I_{DS} R_D$

Where, $V_p = V_{GS\text{-}off}$ & I_{DSS} is Short ckt. I_{DS}

Self-bias
bypassed R_S
[JFET or D-MOSFET]



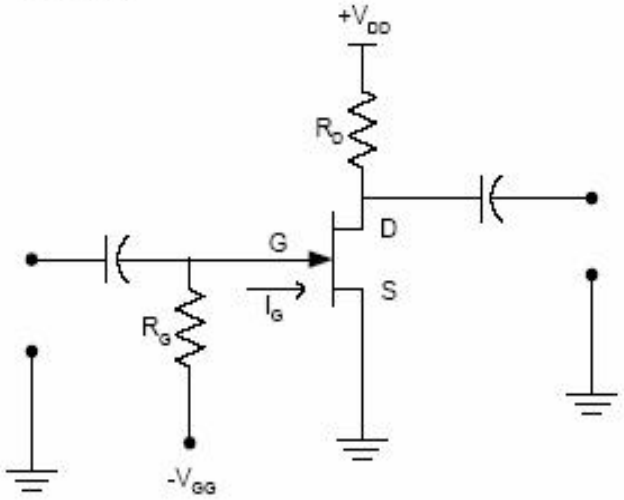
For Self Bias Circuit

$$V_{GS} + I_{DS} R_S = 0$$

$$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$$

JFET Biasing Circuits Cont.

Gate Bias: or Fixed Bias Ckt.



Since $I_G = 0$,

$$V_{GS} = V_{GG}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

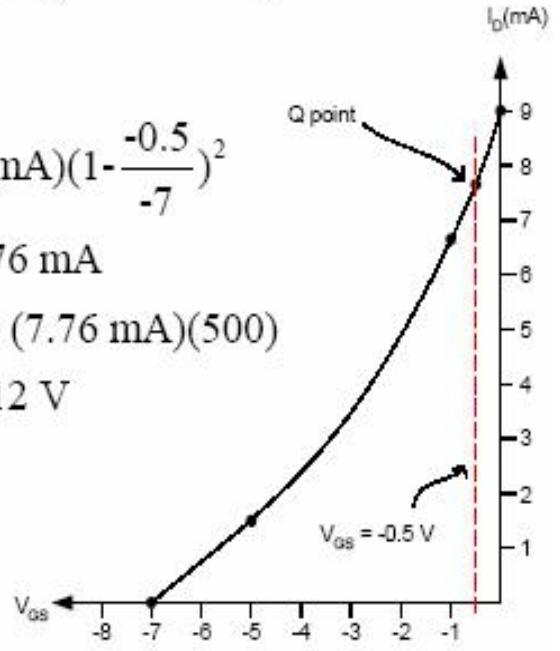
- Example: Determine the Q-point values for the gate biasing circuit if $V_{GG} = -0.5$ V, $V_{GS(off)} = -7$ V, $I_{DSS} = 9$ mA, $V_{DD} = 5$ V and $R_D = 500\Omega$.

$$I_D = (9\text{mA})\left(1 - \frac{-0.5}{-7}\right)^2$$

$$= 7.76 \text{ mA}$$

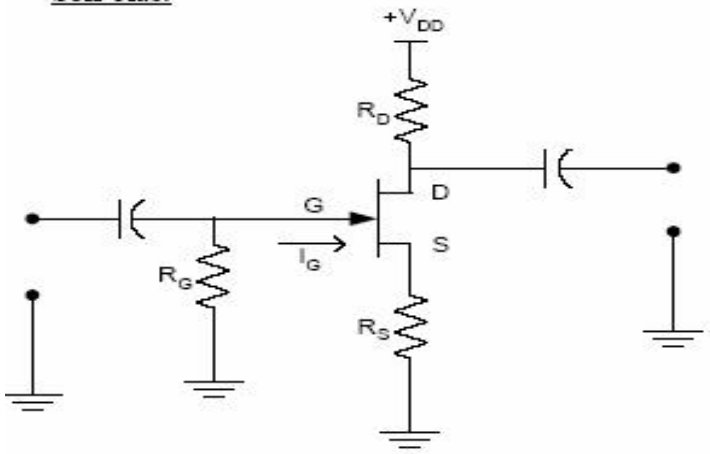
$$V_{DS} = 5 - (7.76 \text{ mA})(500)$$

$$= 1.12 \text{ V}$$



JFET Self (or Source) Bias Circuit

Self bias:



Since $I_G = 0$, $V_G = 0$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

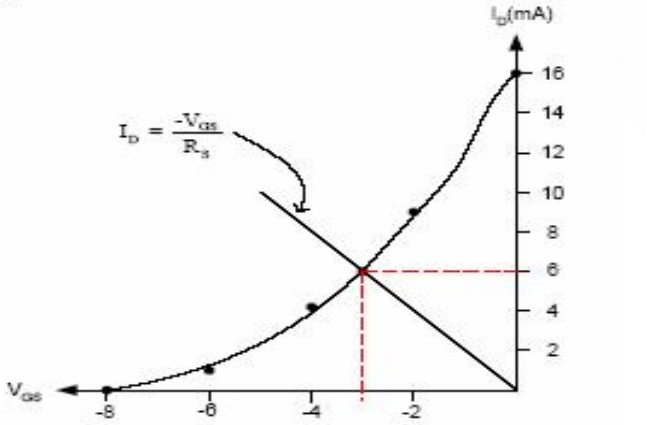
$I_D = \dfrac{-V_{GS}}{R_S}$

$V_{DS} = V_{DD} - I_D(R_D + R_S)$

and $I_{DS} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2$

$\therefore I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = -\dfrac{V_{GS}}{R_S}$

- Example: Determine the Q-point values for the self biasing circuit if $V_{GS(off)} = -8$ V, $I_{DSS} = 16$ mA, $V_{DD} = 10$ V, $R_D = 500\ \Omega$, $R_G = 1$ MΩ and $R_S = 500\ \Omega$.



$I_D = 6$ mA

$V_{DS} = 10 - (6\text{mA})(500+500)$

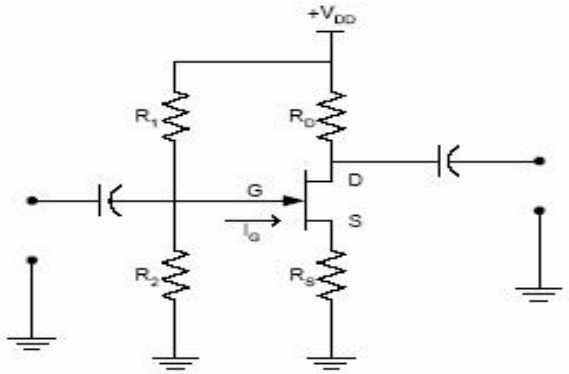
$= 4$ V

$I_{DSS}\left[1 - 2\dfrac{V_{GS}}{V_P} + \left(\dfrac{V_{GS}}{V_P}\right)^2\right] + \dfrac{V_{GS}}{R_S} = 0$

This quadratic equation can be solved for V_{GS} & I_{DS}

The Potential (Voltage) Divider Bias

Voltage-divider bias:



Since $I_G = 0$,

$$V_G = \frac{R_2}{R_1+R_2} V_{DD}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$

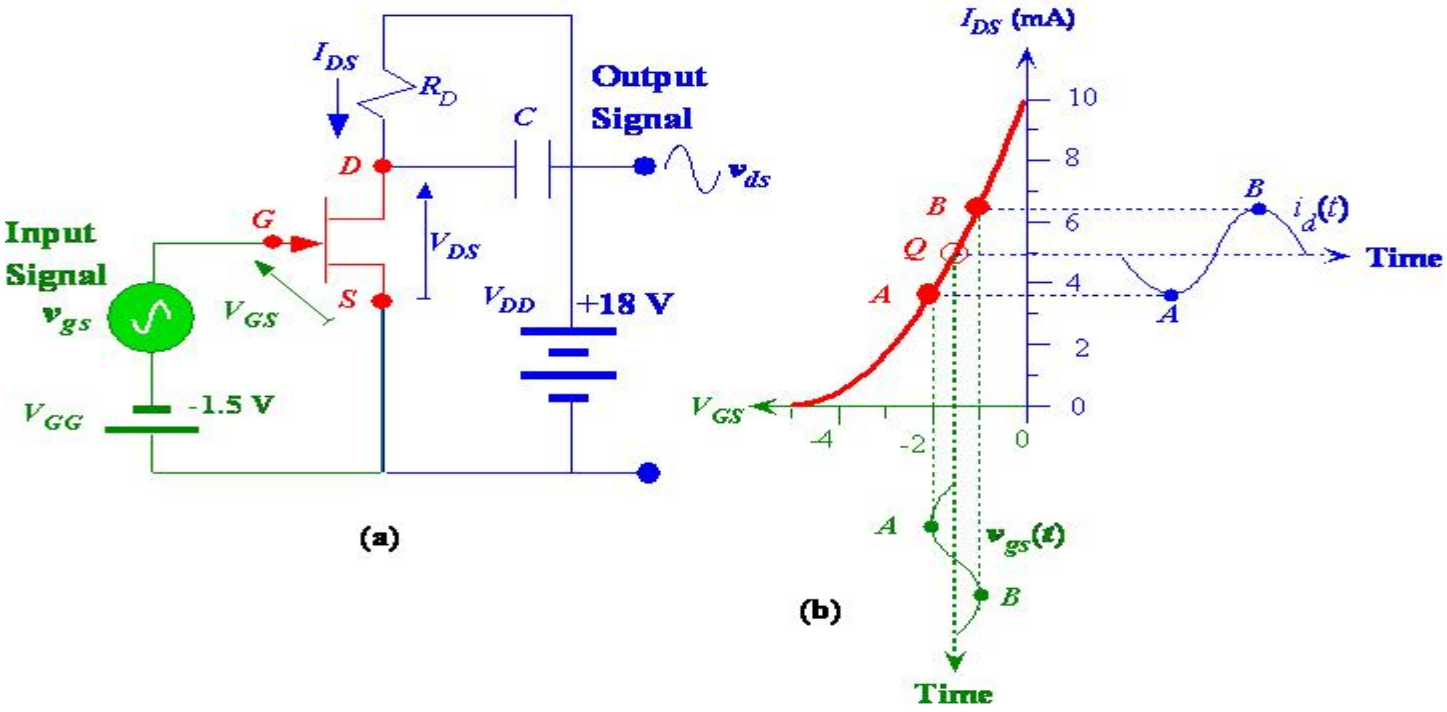
The method used to plot the dc bias line for the voltage-divider bias is as follows:

1. Plot the transconductance curve for the specific JFET.
2. Calculate V_G.
3. Plot V_G on the positive x-axis.
4. Solve for I_D using
$$I_D = \frac{V_G}{R_S}$$
5. Plot I_D found in (4) on the y-axis.
6. Extend the line to intersect the transconductance curve to obtain the Q-point values.

$$\therefore\ I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \frac{V_G - V_{GS}}{R_S} = 0$$

Solving this quadratic equation gives V_{GS} *and* I_{DS}

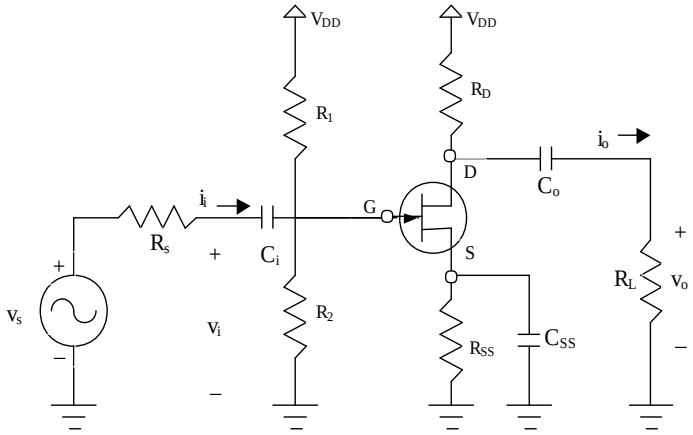
A Simple CS Amplifier and Variation in I_{DS} with V_{gs}



(a) Common source (CS) ac amplifier using a JFET.
(b) Explanation of how I_D is modulated by the signal v_{gs} in series with the dc bias voltage V_{GG}

FET Mid-frequency Analysis:

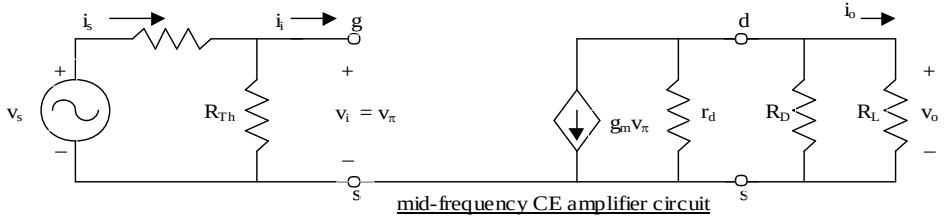
A common source (CS) amplifier is shown to the right.



The mid-frequency circuit is drawn as follows:

- **the coupling capacitors (C_i and C_o) and the bypass capacitor (C_{SS}) are short circuits**
- **short the DC supply voltage (superposition)**
- **replace the FET with the hybrid-p model**

The resulting mid-frequency circuit is shown below.



mid-frequency CE amplifier circuit

Analysis of the CS mid-frequency circuit above yields:

$$A_{vi} = \frac{v_o}{v_i} = -g_m R_L' \text{ , where } R_L' = r_d \| R_D \| R_L$$

$$A_{vs} = \frac{v_o}{v_s} = A_{vi}\left[\frac{Z_i}{R_s + Z_i}\right]$$

$$Z_i = \frac{v_i}{i_i} = R_{Th}, \quad \text{where } R_{Th} = R_1 \| R_2$$

$$A_I = \frac{i_o}{i_i} = A_{vi}\left[\frac{Z_i}{R_L}\right]$$

$$Z_o = \left.\frac{v_o}{i_o}\right|_{\text{seen by } R_L} = r_d \| R_D$$

$$A_p = \frac{p_o}{p_i} = A_{vi} A_I$$

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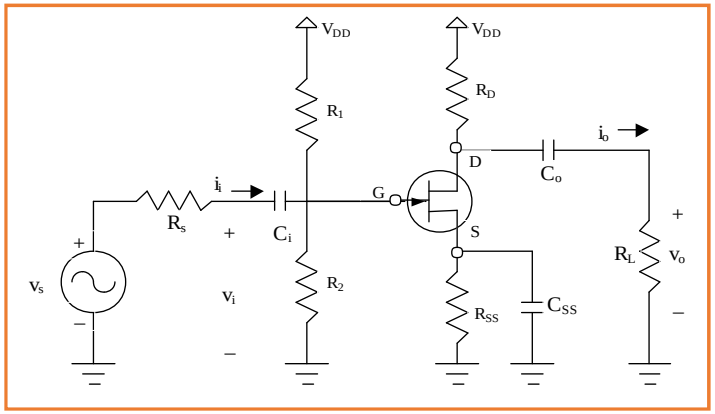

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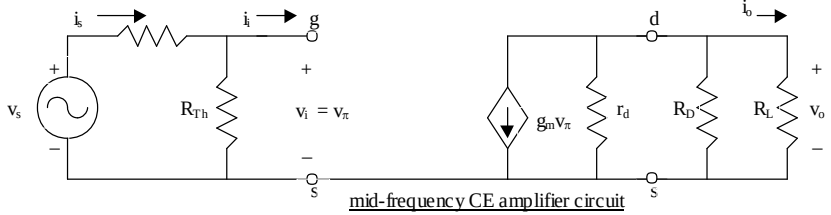

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$$Z_i = \frac{v_i}{i_i} = R_{Th}, \text{ where } R_{Th} = R_1 \| R_2 \qquad A_I = \frac{i_o}{i_i} = A_{vi}\left[\frac{Z_i}{R_L}\right]$$

$$Z_o = \left.\frac{v_o}{i_o}\right|_{\text{seen by } R_L} = r_d \| R_D \qquad A_P = \frac{p_o}{p_i} = A_{vi}A_I$$

Procedure: Analysis of an FET amplifier at mid-frequency:

1) **Find the DC Q-point. This will insure that the FET is operating in the saturation region and these values are needed for the next step.**
2) **Find g_m. If g_m is not specified, calculate it using the DC values of V_{GS} as follows:**

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{V_P^2}\left(V_{GS} - V_P\right) \quad \text{(for JFET's and DM MOSFET's)}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K\left(V_{GS} - V_T\right) \quad \text{(for EM MOSFET's)}$$

(Note: Uses DC value of V_{GS})

3) **Calculate the required values (typically A_{vi}, A_{vs}, A_I, A_p, Z_i, and Z_o. Use the formulas for the appropriate amplifier configuration (CS, CG, CD, etc).**