Arab Academy for Science, Technology & Maritime Transport
School of Engineering
Computer Department
Computing Systems (CC 513)

Midterm No. 1 **Time: 90 minutes**
April, 2007 **Lecturer: Prof. Dr. Magdy Saeb**
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Student Name: …… **ID number: ……**

Answer only four of the following problems:

Problem (1):

1.1 Sketch a table that shows the relation between computational models, language classes and architectural classes.
1.2 Using a schematic, show the difference between concurrency and parallelism.
1.3 A 200,000 instruction benchmark program is run on two processors A and B. Processor A is operating at 600 MHz while processor B is operating at 1.2 GHz.

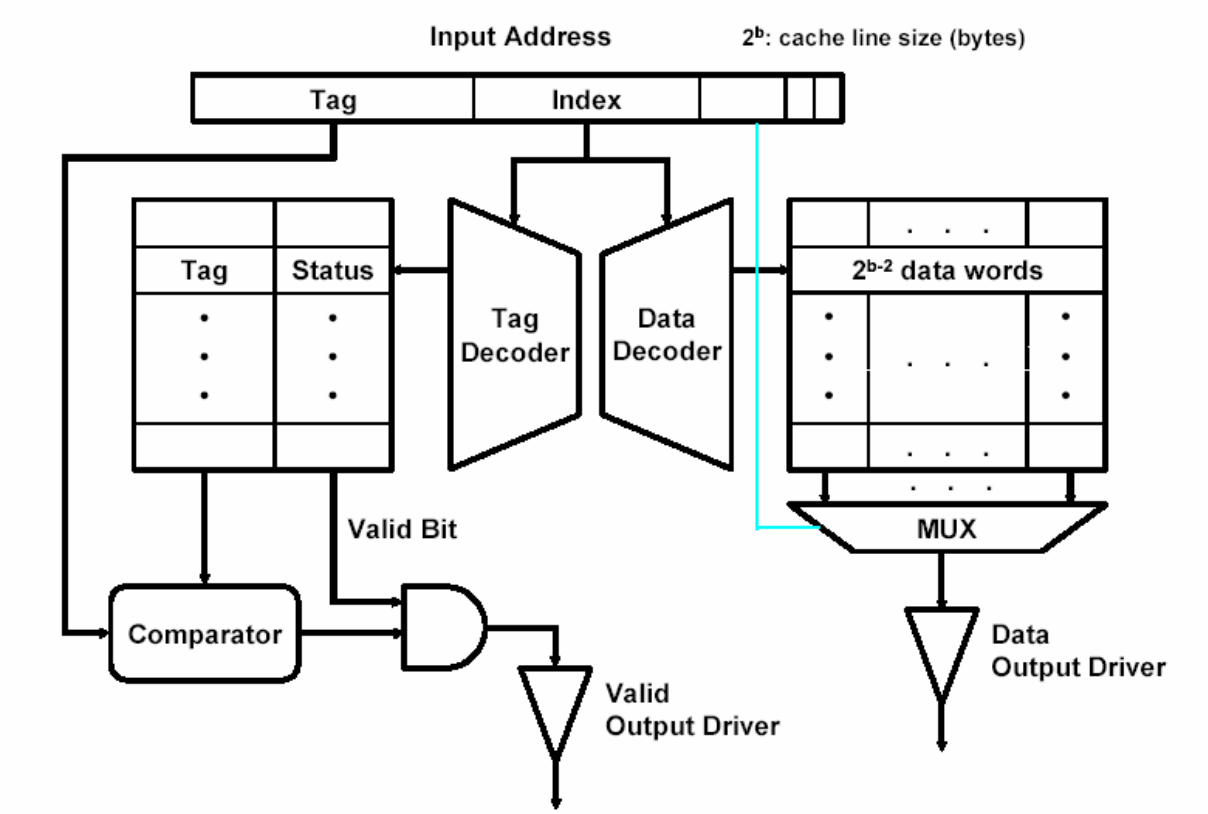
Instruction Type	Instruction Mix	ALU(A) delay in cycles	ALU(B) delay in cycles
Arithmetic	32%	1	2
Data Transfer	36%	2	2
Floating Point	10%	3	4
Control Transfer	22%	2	2

The speed of the memory subsystem remains unchanged, and consequently two clock cycles are needed per memory access in Processor B. Assume 30% of any instruction, except the control transfer type, require one memory access and another 5% require two memory accesses for fetching operands. Do you recommend the upgrade from Processor A to Processor B?

Answer:

Problem 2:

Consider a 256-KB cache with 16word (64-byte) cache lines. The address is 32 bits, and the two least significant bits of the address are ignored since a cache access is word-aligned. The data output is also 32 bits, and the MUX selects one word out of the sixteen words in a cache line. Fill in the table for the direct-mapped (DM) cache shown in figure, using the delay equations given in the table below.



Component	Delay equation (ps)		DM (ps)
Decoder	200×(# of index bits) + 1000	Tag	
		Data	
Memory array	200×$\log_2$ (# of rows) + 200×$\log_2$ (# of bits in a row) + 1000	Tag	
		Data	
Comparator	200×(# of tag bits) + 1000		
N-to-1 MUX	500×$\log_2$ N + 1000		
Buffer driver	2000		
Data output driver	500×(associativity) + 1000		
Valid output driver	1000		

Answer:

Problem 3:

3.1 What are the various types of dependencies encountered in computer programs?

3.2 Consider the following sequence of instructions

```
            Add     #20, R0, R3
            Mul     R3, R2, R3
            Shl     #1,R0
            Branch  LOOP
            Add     R0, R3, R5
            Sub     R2,R3,R6
LOOP        Mov     R3,R4
            Add     R4,R2,R4
```

(a) In all instructions, the destination operand is given last. Initially, register R0 and R2 contain 100 and 50, respectively. These instructions are executed in a computer that has a four-stage pipeline and a data-forwarding mechanism. Assume that the first instruction is fetched in clock cycle 1, and that instruction fetch requires only one clock cycle. Draw a diagram showing the pipeline stages. Describe the operation being performed by each pipeline stage and give the contents of the interstage buffers during each clock cycle.

(b) Suggest how the optimizing compiler can reorder or insert new instructions to achieve better performance on the pipelined processor. Rewrite the above sequence of code as an optimizing compiler would have done while keeping the correct semantics of the program.

Answer:

Problem 4:

4.1 Compute the pipeline performance for an optimum pipeline with k-stages, Ic instructions and frequency f.
A pipelined processor has two branch delay slots. An optimizing compiler can fill one of these slots 85 % of the time and can fill the second slot only 20% of the time. What is the percentage improvement in performance achieved by this optimization, assuming that 20% of the instructions executed are branch instruction?

4.2 Given the processor throughput in instructions per nano second G versus the number of segment partitions S as follows:

$$G = \frac{Performance}{\Delta t}$$

$$G = \frac{1}{(1 + b(S-1))} * \frac{1}{(1+k)\frac{T}{S} + C}$$

Where, b is the frequency of interruptions due to incorrectly guessed or unexpected branches, k is the stretching factor that accounts for clock skew, 0<= k<=1.0, T is the total time in ns, C is the fixed clock over head.
Show that the optimum value of the number of segments partitions to maximize the processor throughput is given by:

$$S_{opt} = \sqrt{(1-b)(1+k)\frac{T}{bC}}$$

Now get S_{opt} given that T = 100 ns, b= 0.2, C = 5 ns, k= 0.125. Also, find G_{max}.

Answer:

Problem 5:

5.1 Using detailed schematics, explain the various architectural differences between VLIW and Superscalar processors.
5.2 One of the major design problems with VLIW architecture is the instruction bandwidth loss due to the reduced number of independent operations that can be issued by an optimizing compiler.

(a) Explain this statement.
(b) Suggest a solution to this problem.

Answer:

Problem 6:

A wafer diameter is 21cm, its cost is $5000, and its defect density 1defect/cm2. The area consumed by one instruction is ai that is approximately equal to 0.01cm2. Find the maximum number of instructions that can be fitted on the processor area (A), such that its cost does not exceed $50.

Hint: The yield (Y) is given by Y = $e^{(-\rho_D A)}$

Answer: