Arab Academy for Science, Technology & Maritime Transport
School of Engineering
Computer Department
Computing Systems (CC 513)

Midterm No. 1 **Time: 90 minutes**
Nov., 2006 **Lecturer: Prof. Dr. Magdy Saeb**
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Student Name: …… **ID number: ……**

Answer all of the following problems:

Problem (1):

1.1 Sketch a table that shows the relation between computational models, language classes and architectural classes.
1.2 Using a schematic, show the difference between concurrency and parallelism.
1.3 A 200,000 instruction benchmark program is run on two processors A and B. Processor A is operating at 600 MHz while processor B is operating at 1 GHz.

Instruction Type	Instruction Mix	CPI (A)	CPI(B)
Arithmetic	32%	1	2
Data Transfer	36%	3	3
Floating Point	10%	3	4
Control Transfer	22%	2	2

(a) Compare the MIPS, throughput and the total execution time of the two processors.
(b) State which instruction type, in your opinion, would positively affect the performance of the two processors if the designers worked on improving it. Please justify your answer.

Answer:

Problem 2:

2.1 Using detailed schematics, explain the various architectural differences between VLIW and Superscalar processors.

2.2 Consider a program segment consisting of 15 instructions. The cache consists of blocks each can hold up to 6 instructions only. Assume the cache is empty at the beginning of execution and that the instruction queue can hold up to four instructions. The instruction fetch unit reads two instructions at a time from the cache and the cache miss penalty is three cycles. Draw a timing diagram showing the size of the prefetch buffer at each cycle

Answer:

Problem 3:

3.1 What are the various types of dependencies encountered in a computer programs?

3.2 Consider the following sequence of instructions

```
Add   #20, R0, R2
Mul   #3, R2, R3
And   #$3A, R2, R4
Add   R0, R3, R5
```

In all instructions, the destination operand is given last. Initially, register R0 and R2 contain 100 and 50, respectively. These instructions are executed in a computer that has a four-stage pipeline. Assume that the first instruction is fetched in clock cycle 1, and that instruction fetch requires only one clock cycle.

Draw a diagram showing the pipeline stages. Describe the operation being performed by each pipeline stage and give the contents of the interstage buffers during each of clock cycles 1 through 5.

3.3 Repeat 3.2 and assume that the register file allows two write steps to proceed in parallel. How would you use additional storage buffers to make it possible for delayed instructions to proceed earlier. Draw a block diagram your improvements.

Answer:

Problem 4:
The speed up of a parallel algorithm is defined as the time taken in a serial execution divided by that taken in a parallel architecture. Calculate the speed up of a vector floating-point addition between two vectors of 128 elements each on a vector processor with a floating-point addition pipeline unit that is six stages long. Take α as the number of stages, γ as the stage duration in seconds, and n as the number of vector elements.

Answer: