Section 9.2: 8088/ 8086 Microprocessor

13.

Point of comparison	8086	8088
External data bus	16 bit	8 bit
Address bus	AD0→ AD15 for address/data	AD0→ AD7 for address/data A8→A19 for addresses only

14. ALE is an ***output*** signal for the 8088/ 8086
15. What is the maximum number of byte of memory addressable by the 8088/ 8086 and why?

    1 M since the 8088/ 8086 has 20 bit address lines so $2^{20} = 1M$
16. Reset is an input signal for the 8088/ 8086.
17. When the 8088/86 uses the pins for addresses, they are output, but when they are used for data, they will be ***both in and out***.
18. To use a math coprocessor with the 8088/ 8086, one must connect the 8088/ 8086 in ***maximum mode.***
19. An address must be latched from pins AD0-AD7 in the 8088. ***True***
20. Which of the following signals is provided by the 8088 CPU in minimum mode?

    ALE

    { EMBED Equation.3 }

    { EMBED Equation.3 }
21. What is the advantage of Demultiplexing address/data in the 8088/86 CPU?

    The process of separating the address and data from pins AD0-AD15 in 8086, from pins AD0-AD7 in 8088. This has the advantage of minimizing the number of external pins.
22. What is the penalty (disadvantage) in terms of clocks in Problem 21?

    T1
23. ALE is activated in which T state?

    T1

25. To use the 8088/86 with the 8087 math coprocessor, is the minimum/ maximum pin connected to low or high?

    Low

26. When the input signal RESET is activated, what are the contents of the IP and CS registers?

    IP=0000H; CS=FFFFH

Section 9.3: 8284 Clock Generator and driver

27. In the 8284, a crystal frequency of 10 MHz is used calculate the following output frequencies
    (a) OSC = frequency of crystal = 10 MHz
    (b) CLK= { EMBED Equation.3 }frequency of the crystal= 3.33 MHz
    (c) PCLK={ EMBED Equation.3 } frequency of the crystal={ EMBED Equation.3 }.
28. If a given 8088 system needs to work with a frequency of 8 MHz, what must be the crystal frequency of the 8284?

    The crystal frequency equal 3 times the system frequency = 24MHz

Section 9.4: 8288 Bus Controller

29. If the CPU provides the status signals S0=0, S1=1, and S2=1 to the 8288, which control signals are activated?

    Write memory.

30. 8288
31. a, c, e, f
32. b
33. c
34. a

Section 9.5: IBM PC/XT BUSES

35. 8088/86
36. 3 chips
37. 8088 CPU, DMA
38. a. bidirectional bus buffering 74X245
    b. unidirectional bus buffering 74X244
39. d
40.
41. 8284(D,F), 8088(a,g), 8288(C, E)
42. DIR= HIGH, G= LOW
43. DIR= LOW, G=HIGH
44. ISOLATION
45. a
46. G=High, OE=LOW